

# Calculation of PCB Power Loop Stray Inductance in GaN or High di/dt Applications

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**Abstract**—This paper is concerned with the determination of parasitic inductance values in very fast switching power devices. To keep improving today's power converters, new technologies are studied which exhibit very low switching times. The wide band gap semi-conductors are among the key aspects of these improvements. Thanks to their internal properties, they allow very fast di/dt and dv/dt with very small footprint. Stray loop inductance needs to be kept low, as it creates high peak voltage upon switching of a transistor with fast di/dt. In particular, the stray inductance value with respect to the loop size and geometry needs to be calculated accurately at the design stage of the power converters. This paper analyzes three loop geometries and studies one with minimized stray inductance and optimal current distribution. An analytical method is proposed, which uses Biot-Savart law for an accurate analytical estimation of the magnetic field intensity in the selected geometry, leading to inductance calculation. A comparison between the classical two-plate inductance estimation formula and the proposed stray inductance estimation is presented, proving more accurate value with the method proposed in the paper. Finally, an experiment has validated the new inductance estimation formula.

**Index Terms**—Power Electronics, Fast Switching, Modeling, GaN, Design of Power Converters.

## I. INTRODUCTION

The evolution of power electronics is tightly correlated to the improvements in the semiconductor technology, the use of new material and fabrication process, which all look for higher compacity, higher efficiency and lower cost [1]. Wide Band Gap (WBG) components like GaN semiconductors offer the possibility of switching currents in the range of 10 A and voltages up to 650 V with 1 to 2 ns rise times while keeping the cost low. These very short switching times offer the possibility of decreased switching losses for MHz-range switching frequencies [2].

In many applications, the switching topology makes proper use of a low-side/high-side half-bridge configuration as the one

depicted in Fig. 1. As the switching current must flow through copper material on a geometry (printed circuit board (PCB) tracks or wires) characterized by a loop area  $A$  and a loop length  $l$ , joule losses through the PCB tracks and inductance due to the magnetic field created by the loop are inevitable. These two behaviors can be modeled by lump resistance and inductance. Thus, the inductance  $L_{pcb}$  and resistance  $R_{pcb}$  forming the power loop, which also includes the half-bridge and the DC voltage source as shown Fig. 1.

More specifically,  $L_{pcb}$ ,  $R_{pcb}$ , and the switches internal capacitors and packaging inductance  $L_{Q1,Q2}$  are the parameters causing unwanted behaviors like overvoltage, ringing [3], [4], parasitic losses and ultimately breakdown [5]. This phenomenon is illustrated in Fig. 2 where a LTSpice® simulation is conducted with a half-bridge circuit made of two very fast GaN transistors. Two values of PCB inductance (9.42 nH and 1.35 nH) have been simulated and reported. The first one shows a peak voltage/bus voltage ratio of 2.2, where the component maximum voltage rating of 100 V would be exceeded with an important overvoltage and ringing which would lead to the component breakdown. The second one

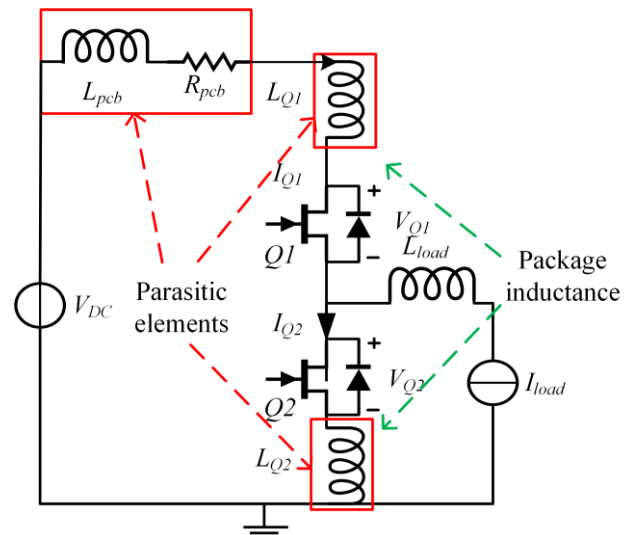


Fig. 1. Power arm with an inductive load,  $L_{pcb}$  and  $R_{pcb}$  are the conductor parasitic elements.

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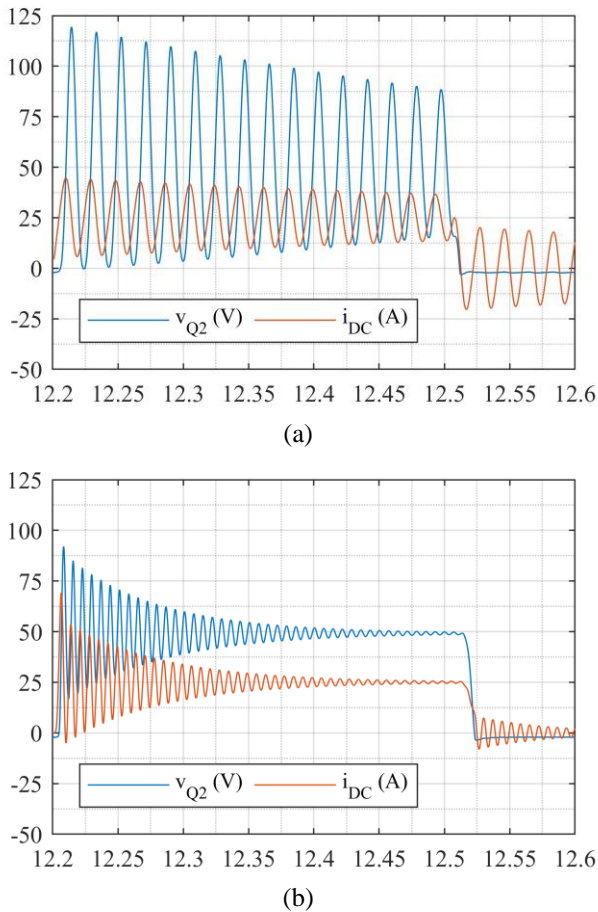


Fig. 2. Switching waveform of the component EPC2022 GaN transistor simulated with LTSpice®, (a) is for  $L_{pcb} = 9.42$  nH, (b) is for  $L_{pcb} = 1.35$  nH. Input DC voltage  $V_{DC} = 50$  V, load current  $I_{load} = 25$  A.

displays a peak voltage/bus voltage ratio of 1.3, with lower overvoltage and ringing, keeping the switch under its maximum voltage value thanks to a lower stray inductance.

In past literature, a few methods have been developed to control and mitigate these parasitic elements [6], [7]. Some of them aim at minimizing the current loop area and the current path length. Other designs intend to minimize the generated flux by using nullifying methods. Even though results were obtained for reducing the overvoltage and losses [8], difficulty remains for evaluating the power loop stray inductance without numerical simulations [9], [10], [11]. The present work aims to be complementary with the previous works by providing a way to easily calculate the PCB stray inductance for a defined loop shape without using Finite Element Analysis (FEA) or experimental tests.

Going from the current loop physical dimensions to the values of  $L_{pcb}$  and  $R_{pcb}$ , which in turn will lead to the overvoltage across  $Q_1$  and  $Q_2$  without the use of a numerical simulation is a difficult task.

The lump inductance of a loop formed by two parallel plates (e.g. the top and bottom copper plates of a PCB) can be obtained by using (1) which serves as a useful approximation in many cases [12].

$$L_{pcb} = \mu_0 \frac{e}{w} l \quad (1)$$

where  $e$  is the distance between the upper and lower conducting plates,  $w$  is the width of these conducting plates and  $l$  is the length of the conducting planes.

As will be shown in the paper, (1) can be used under certain assumptions. However, the latter becomes inaccurate for low values of the  $w/e$  ratios, which are characteristic of the geometrical dimensions of very small switches used with GaN semiconducting material.

The present paper will discuss the PCB positioning of GaN transistors with a closer investigation at three possible layouts for the copper tracks forming the current loop from the decoupling capacitor to the half-bridge. The best suited geometry will be identified and a mathematical development using Biot-Savart law will be proposed for estimating the loop inductance  $L_{pcb}$  with accuracy. The result is validated with experimental and numerical simulation tools. A simplified expression, giving a similar result within a known error range is given and compared to the classical approximation equation.

The paper shows a comparison between different topologies. The one most adapted to the current problem of fast switching is then analytically studied. During a converter design procedure, choices must be made for the power components and thus for the power loop dimensions. Many software like Q3D Extractor or Magnet can be used to model the conductors and numerically find the inductor value. The current work aims to provide a solution giving the inductance depending on the power switch size without the need for finite-element simulation. It then becomes possible to test many configurations without the need for 3D modelling and simulation. To obtain high accuracy, a FEA software needs to work by using a fine mesh. For very high frequencies, the skin effect is very thin, implying a very fine mesh. This is time consuming and adds up to the total time if you want to test many configurations.

A rough estimation on the time needed to test one configuration using 3D FEA is of one hour. Of course, it depends on the user's skills and computer speed. In any case, the FEA simulation is much longer than using analytical expressions where the result is immediate. Moreover, the simplified equation allows it to be integrated in scripts while the co-simulation can be complicated and time consuming when used.

The paper is organized as follows: section II presents the three PCB layouts investigated for reducing  $L_{pcb}$ . Section III presents the analytical derivation of  $L_{pcb}$  for the case of the two-plate current loop. FEA validation of the obtained expression is presented in section III. Section IV proposes a novel expression for estimating the loop inductance. Section V presents a practical demonstration of the switching behavior with the loop geometry selected. Finally, section VI gives a conclusion to the paper.

## II. ANALYSIS OF THREE POWER LOOP CONFIGURATIONS

GaN-based power transistors exhibit very high-power density. Thanks to the material properties, high voltages and currents can be switched in the ns range, while keeping the chip

extremely small. Fig. 3 shows the size difference between two transistors package for a given voltage rating. A standard silicon (Si) D<sup>2</sup>PAK MOSFET package is shown, with a much larger footprint than the GaN HEMT (High Electron Mobility Transistor), which enables low parasitic inductance.

Apart from the power loop PCB inductance, the transistor package leads are themselves a source of parasitic inductance, adding all of them together is the so called stray inductance. When comparing the packages, numerous differences appear, which have an impact on the circuit stray inductance. The standard D<sup>2</sup>PAK exhibits a package inductance varying between 5 nH and 7 nH [13], [14] while the package proposed by the GaN transistor manufacturer EPC is given in the 0.1 nH range for a size of 3.5x1.4 mm. This low package stray inductance is key in minimizing the overall power loop inductance.

The direct consequence of an important reduction in size is the reduction of the width of the copper conductor and the related magnetic flux produced by the power loop when carrying the rated current. Hence, the underlying assumption behind (1) is no longer valid. In this section, the three loops studied with the assumption of very small footprint will use the results from FEA to properly estimate the corresponding loop stray inductance.

The following subsections will study the various loop geometries proposed in past literature, such as the U-shape, the Top-Bottom and the Top-Inner power loops, with the objective of reducing the magnetic flux area created by the loop. Three main topologies exist and exhibit different results [15].

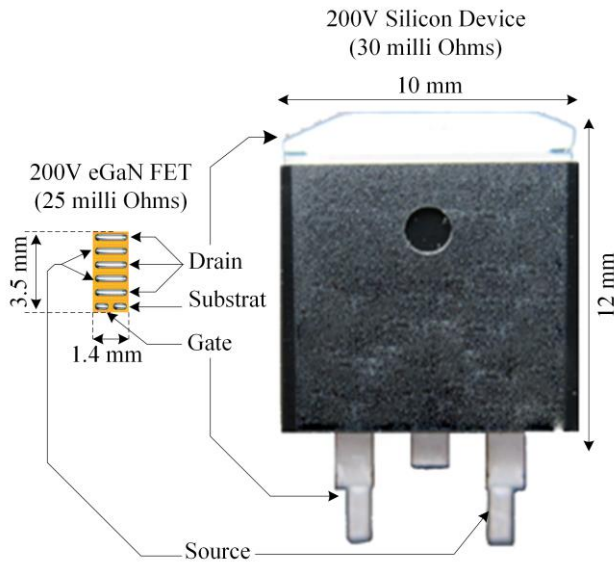


Fig. 3. Comparison of a D<sup>2</sup>PAK standard packaging to EPC2010C, a 200 V, 22 A transistor. (Source: [www.http://epc-co.com](http://epc-co.com)).

#### A. U-shape Power Path

The U-shape power path has been discussed in a number of publications [6], [16] and is illustrated by Fig. 4(a). This concept aims at making the current loop area as small as possible and at the same time keeping it on one side of the PCB. This solution is easy to implement and has the cost and

fabrication advantages of a single-sided PCB. The resistive path exhibits low resistance value  $R_{pcb}$ . However, the loop parasitic inductance  $L_{pcb}$  will be a concern in the case of high di/dt switching. This is mainly due to the center magnetic flux created upon the circulation of a current in the power loop. The current density distribution  $J$  and field  $H$  are computed with FEA and displayed in Fig. 4 as well.

Fig. 4 shows another aspect that needs to be carefully investigated when dealing with  $R_{pcb}$  and  $L_{pcb}$ : the skin effect behaviour observed in the power loop. Fast switching transistors like GaN HEMT or Ultra-Fast MOSFETs are intended to be used in Switch-Mode Power Supplies (SMPS) with 1 MHz-range switching frequency. Moreover, the ringing phenomenon observed across the transistor at turn-off involves voltage and current oscillations in the 100 MHz range, as it was shown in Fig. 2.

As the effect of the stray inductance and  $L_{pcb}$  is to affect the circuit during such very fast transition periods, our analysis must consider the skin effect behavior.

As shown in Fig. 4 for a 1 MHz frequency, the current density is higher in the inner part of the U, where the magnetic field is also stronger. The current is unevenly distributed at 1 MHz, making a poor use of the copper material when carrying high current values. This current distribution will also lead to the switches heating unevenly. The resulting values are a loop inductance  $L_{PCB} = 9.4$  nH and a loop resistance of  $R_{PCB} = 2.2$  m $\Omega$ .

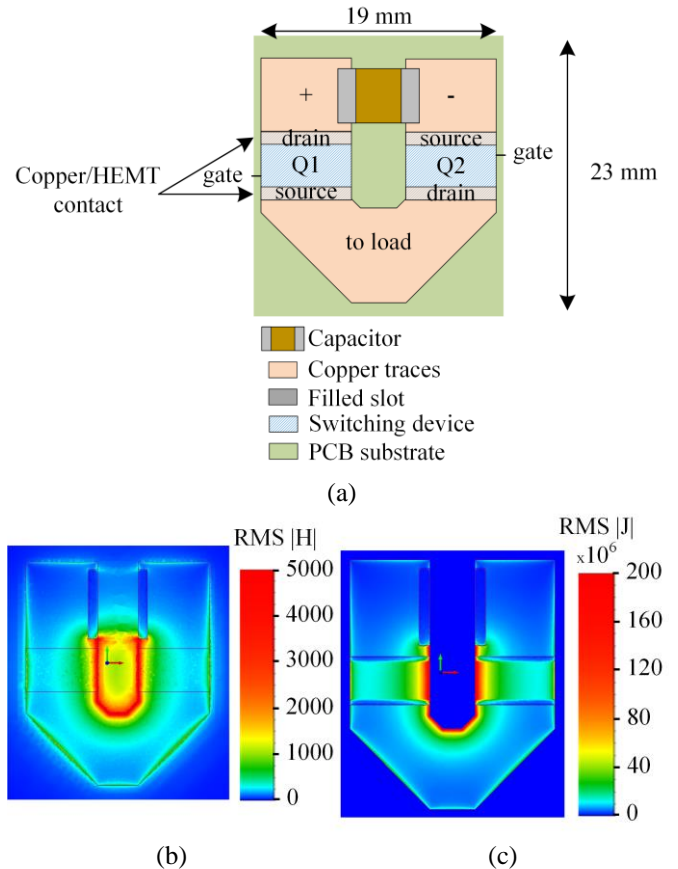


Fig. 4. (a) U-Shaped topology (b)  $|H|$  field produced by the circulating current (c) current density  $J$ . Current amplitude 10 A, frequency 1 MHz. The loop is 19x23 mm.



### B. Top-Bottom Power Path

This method consists in mirroring the current path located on the top layer of a PCB by implementing a symmetrical current path on the PCB bottom layer. This forms a symmetry plan orthogonal to the switches leading to a reduced area for the circulation of the magnetic flux. This topology is illustrated in Fig. 5(a). Since two layers are involved, the inter-layer connections must be considered with extra care. The standard manufacturing process does not allow for an exact control of the *vias* manufacturing. A different method is chosen for this study; a slot is designed at each end of the traces, instead of *vias* and then filled with soldering tin.

This way it can be considered as a metal conductor where all the parameters are known. The flux surface area is diminished, leading to a lower inductance. The FEA results are shown Fig. 5(b), (c) where the current density appears well distributed, lowering its maximal value compared to the U-shaped topology.

In the geometry of Fig. 5, with a PCB thickness of  $e = 1.6$  mm the obtained inductance is  $L_{pcb} = 3.56$  nH and the 1 MHz resistance is  $R_{pcb} = 1.6$  m $\Omega$ . This result shows a great improvement compared to the U-shaped method, with an inductance reduction of 62% and a resistance reduction of 27%.

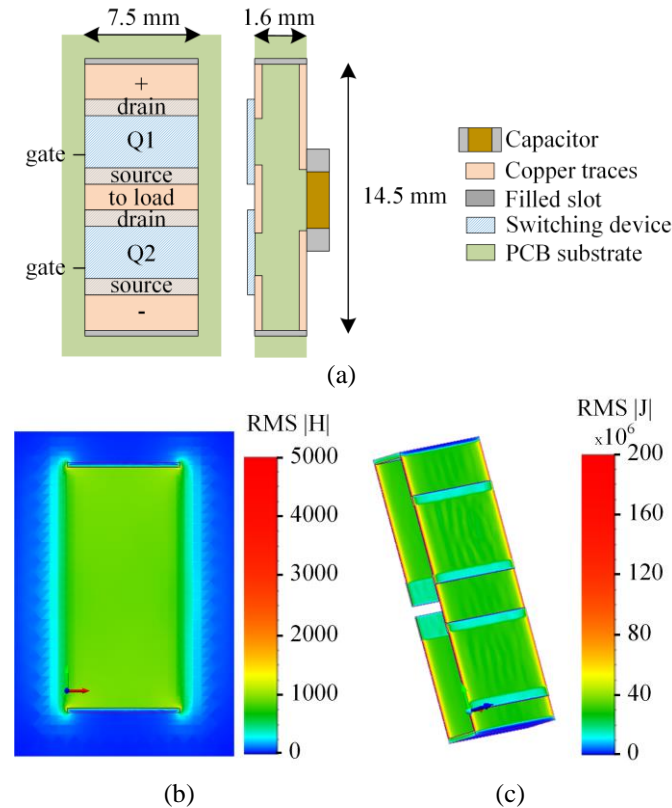


Fig. 5. (a) Top-bottom topology with a 1.6 mm PCB (b)  $|H|$  field produced by the circulating current (c) current density  $J$ . Current amplitude 10 A, frequency 1 MHz. The loop is 7.5x14.5 mm

### C. Internal Layer Power Path

This method is similar to the Top-Bottom method, with the exception of using a multi-layer PCB, in which an internal layer is used for the current return instead of the PCB bottom layer.

This allows further reducing the loop area. The topology is shown in Fig. 6(a) and the FEA results in Fig. 6(b), (c). As for the Top-Bottom topology, the current density is well distributed along the copper width with an even smaller flux loop area. The results presented here are for a 1.6 mm PCB thickness with 2 internal layers equally spaced. Thus, the spacing between the two flat conductors is one third of the PBC thickness, that is  $e = 0.53$  mm.

The FEA calculation gives an inductance of  $L_{pcb} = 1.35$  nH and a 1 MHz resistance of  $R_{pcb} = 0.95$  m $\Omega$ . The stray inductance is reduced by 62% and the resistance by 40% compared to the previous method (section II.B.). The result can be further improved by using a thinner PCB with more layers. This configuration shows the lowest inductance value and an evenly distributed current, allowing equal heat distribution. These two parameters make it ideal for the present study.

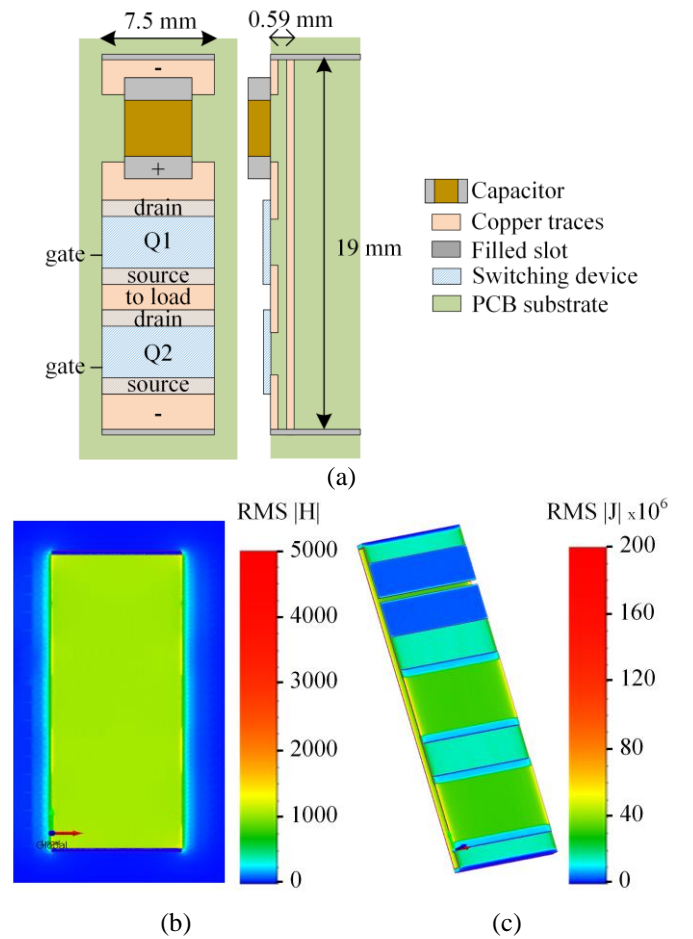


Fig. 6. (a) Optimized topology using an internal layer, (b)  $|H|$  field produced by the circulating current, (c) current density  $J$ . Current amplitude 10 A, frequency 1 MHz. The copper conductor is 7.5 mm wide and 19 mm long. Spacing between the two conductor plates is 0.59 mm.

### III. INTERNAL LAYER POWER PATH INDUCTANCE CALCULATION

#### A. Modeling Methods

To determine the values of  $L_{pcb}$ , one of the most popular method is to use FEA software where the PCB layout is imported from the PCB design software. This is the method that was used in section II. A faster method is to approximate it by a broad side tracks inductance with the limits that the width must be greatly higher than the distance between the conductors. Then (1) is applied to the internal layer topology displayed in Fig. 6.

All these methods are valid, but the cons are that either the obtained value is approximated with an unknown error or a long and fastidious simulation must be set and solved. To obtain a better approximation that does not suffer the limits given previously, a new analytical development for modeling the value of  $L_{pcb}$  is presented in this paper. The analytical development is based on the Maxwell's equations and the Biot-Savart law. Then a novel estimation formula is derived and compared to the classical one.

#### B. Application of Maxwell and Biot-Savart Laws

Considering the skin and proximity effect, the considered conductor height should be no more than the skin depth defined by (2).

$$\delta = \sqrt{\frac{1}{\pi f \mu_0 \sigma_{Cu}}} \quad (2)$$

Then, the current density  $J$  is considered constant inside the conductor height  $\delta$  and we will make the simplifying assumption of  $h = \delta$  for the presented mathematical development. Fig. 7 shows two cases: 1) copper thickness superior to the skin depth and 2) for a thickness equal to the skin depth. The second case allows us to consider  $J$  constant and will be used for the mathematical development.

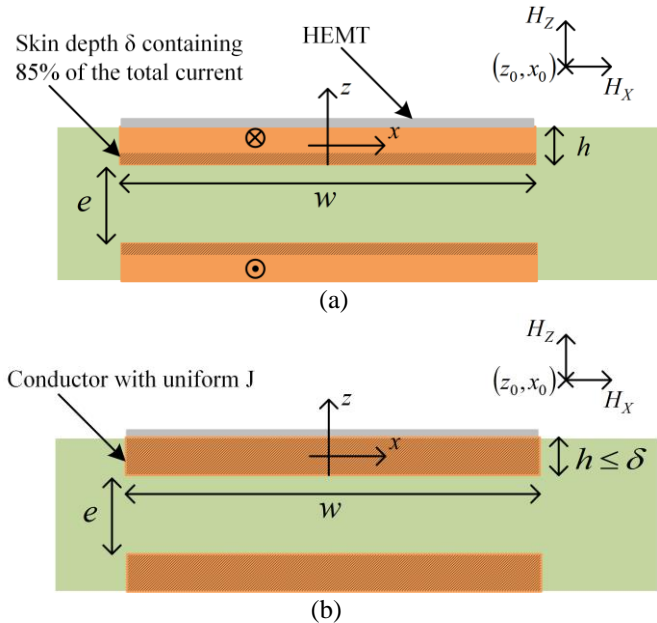


Fig. 7. Skin depth effect and its consideration for the analytical development. (a) is when the considered thickness  $h > \delta$  and (b) is for  $h \leq \delta$ .

Where  $f$  is the frequency of the signal considered (typically 300 MHz during the ringing phenomenon),  $\mu_0$  is the void permittivity and  $\sigma_{Cu}$  is the conductivity of copper.

It is then possible to use Biot-Savart law [17] to retrieve the  $H$  field and associated magnetic flux  $\phi$  for one conductor and use (3) to obtain the value of the stray inductance  $L_{pcb}$ , based on the current  $I_{pcb}$  and the number of turns  $n$ . In the present case,  $I_{pcb}$  is assumed as a constant value, flowing in the thickness determined by the skin depth, as detailed above,  $n = 1$  and the flux  $\phi$  is calculated in between the two conductors of Fig. 7. The coordinates referential and axis used in this analysis are laid out as described in Fig. 7.

$$L_{pcb} = \frac{n\phi}{I_{pcb}} \quad (3)$$

The Biot-Savart law is used, in order to provide the  $H$  field for any specified point depending on the current density and geometry. Applied to our problem geometry we need to solve (4) giving the field at any point  $(x_0, z_0)$  around the conductor.

$$\vec{B}(\vec{r}_0) = \frac{\mu_0}{4\pi} \iiint_{V_{conductor}} \frac{\vec{J}_s(\vec{r}) \times (\vec{r}_0 - \vec{r})}{|\vec{r}_0 - \vec{r}|^3} dxdydz \quad (4)$$

The coordinates  $(x_0, z_0)$  are associated to vector  $\vec{r}_0$ , whereas coordinates  $(x, z)$  are associated to vector  $\vec{r}$ , which defines any given point inside the conductor. The Biot-Savart law formulated by (4) considers a surface current density vector  $\vec{j}_s$ , which has a constant value  $J$  and orientation over the entire conductor volume  $V_{conductor}$ , that is, inside the conductor between the boundaries  $-w/2 < x < w/2$  and  $-h/2 < z < h/2$ . Vector  $\vec{j}_s$  is oriented parallel to the  $y$ -axis in the upper conductor and anti-parallel to the  $y$ -axis in the bottom conductor. Given  $\vec{j}_s$  orientation, the magnetic field at any point will have an  $x$ -axis component  $H_x$  and a  $z$ -axis component  $H_z$ , with no  $y$ -axis component. As the parallel conductors extend in the  $y$ -axis from  $y = -\infty$  to  $y = +\infty$ , we can demonstrate (5):

$$\int_{-\infty}^{+\infty} \frac{1}{\left(\sqrt{(x_0 - x)^2 + (y_0 - y)^2 + (z_0 - z)^2}\right)^3} dy = \frac{-2}{(x_0 - x)^2 + (z_0 - z)^2} \quad (5)$$

Inserting (5) into (4), the upper conductor will create a field  $H_{upper}$ :

$$\begin{cases} H_{upperX}(x_0, z_0) = \frac{J}{2\pi} \int_{-w/2}^{w/2} \int_{-h/2}^{h/2} \frac{z_0 - z}{(z_0 - z)^2 + (x_0 - x)^2} dz dx \\ H_{upperY}(x_0, z_0) = 0 \\ H_{upperZ}(x_0, z_0) = \frac{-J}{2\pi} \int_{-h/2}^{h/2} \int_{-w/2}^{w/2} \frac{x_0 - x}{(z_0 - z)^2 + (x_0 - x)^2} dx dz \end{cases} \quad (6)$$

where the current density in the top and lower conductor  $J$  is given by (7).

$$J = \frac{I}{wh} \quad (7)$$

The solution for the  $H$  field generated at each point  $(x_0, z_0)$  in the space around the conductors is detailed in Appendix I, giving (8) as a solution.

$$\begin{aligned}
 H_{upperX}(x_0, z_0) = & \frac{J}{4\pi} \left[ (2z_0 - h) \tan^{-1} \frac{2w(h - 2z_0)}{(h - 2z_0)^2 - w^2 + 4x_0^2} \right. \\
 & + (2z_0 + h) \tan^{-1} \frac{2w(h + 2z_0)}{(h + 2z_0)^2 - w^2 + 4x_0^2} \\
 & - (w/2 - x_0) \ln \frac{(w - 2x_0)^2 + (h - 2z_0)^2}{(w - 2x_0)^2 + (h + 2z_0)^2} \\
 & \left. - (w/2 + x_0) \ln \frac{(w + 2x_0)^2 + (h - 2z_0)^2}{(w + 2x_0)^2 + (h + 2z_0)^2} \right] \\
 H_{upperZ}(x_0, z_0) = & \frac{-J}{4\pi} \left[ (2x_0 - w) \tan^{-1} \frac{2h(w - 2x_0)}{(w - 2x_0)^2 - h^2 + 4z_0^2} \right. \\
 & + (2x_0 + w) \tan^{-1} \frac{2h(w + 2x_0)}{(w + 2x_0)^2 - h^2 + 4z_0^2} \\
 & - (h/2 - z_0) \ln \frac{(w - 2x_0)^2 + (h - 2z_0)^2}{(w + 2x_0)^2 + (h - 2z_0)^2} \\
 & \left. - (h/2 + z_0) \ln \frac{(w - 2x_0)^2 + (h + 2z_0)^2}{(w + 2x_0)^2 + (h + 2z_0)^2} \right]
 \end{aligned} \quad (8)$$

Similarly, the lower conductor will create a field  $H_{lower}$

$$\begin{cases}
 H_{lowerX}(x_0, z_0) = \frac{-J}{2\pi} \int_{-w/2}^{w/2} \int_{-h/2}^{h/2} \frac{z_0 - z}{(z_0 - z)^2 + (x_0 - x)^2} dz dx \\
 H_{lowerY}(x_0, z_0) = 0 \\
 H_{lowerZ}(x_0, z_0) = \frac{J}{2\pi} \int_{-h/2}^{h/2} \int_{-w/2}^{w/2} \frac{x_0 - x}{(z_0 - z)^2 + (x_0 - x)^2} dx dz
 \end{cases} \quad (9)$$

Which accepts (10) as a solution. Naturally, the total field is the sum of (8) and (10) at any point.

The field generated by two conductors can now be calculated analytically for each desired coordinate  $(x_0, z_0)$  with the resulting  $H$  field displayed in Fig. 8, with the geometrical parameters conductor width  $w = 7.5$  mm, thickness  $h = 35$   $\mu$ m, spacing  $e = 0.42$  mm. The calculation is done for a current  $I = 10$  A. As a comparison, a 2-D FEA was also performed on the exact same geometry with the results shown in Fig. 9. The obtained field is the same in both distribution and intensity in both analytical computation and FEA.

$$\begin{aligned}
 H_{lowerX}(x_0, z_0) = & -\frac{J}{4\pi} \left[ (2(z_0 + e) + h) \tan^{-1} \frac{2w(-h - 2(z_0 + e))}{(-h - 2(z_0 + e))^2 - w^2 + 4x_0^2} \right. \\
 & + (2(z_0 + e) + 3h) \tan^{-1} \frac{2w(3h + 2(z_0 + e))}{(3h + 2(z_0 + e))^2 - w^2 + 4x_0^2} \\
 & - (w/2 - x_0) \ln \frac{(w - 2x_0)^2 + (-h - 2(z_0 + e))^2}{(w - 2x_0)^2 + (3h + 2(z_0 + e))^2} \\
 & \left. - (w/2 + x_0) \ln \frac{(w + 2x_0)^2 + (-h - 2(z_0 + e))^2}{(w + 2x_0)^2 + (3h + 2(z_0 + e))^2} \right] \\
 H_{lowerZ}(x_0, z_0) = & \frac{J}{4\pi} \left[ (2x_0 - w) \tan^{-1} \frac{2h(w - 2x_0)}{(w - 2x_0)^2 - h^2 + 4(z_0 + e + h)^2} \right. \\
 & + (2x_0 + w) \tan^{-1} \frac{2h(w + 2x_0)}{(w + 2x_0)^2 - h^2 + 4(z_0 + e + h)^2} \\
 & + (h/2 + (z_0 + e)) \ln \frac{(w - 2x_0)^2 + (-h - 2(z_0 + e))^2}{(w + 2x_0)^2 + (-h - 2(z_0 + e))^2} \\
 & \left. - (3h/2 + (z_0 + e)) \ln \frac{(w - 2x_0)^2 + (3h + 2(z_0 + e))^2}{(w + 2x_0)^2 + (3h + 2(z_0 + e))^2} \right]
 \end{aligned} \quad (10)$$

As expected, this result shows that the field is concentrated between the two conductors, due to the currents going in opposite ways on the top and bottom conductors. The field becomes nearly null outside the inner space and concentrated inside. The analytical formulations of (8) and (10) will be of great value for considering the end effect, which show some variation in the field intensity and will require careful consideration for low geometrical ratios  $w/e$ . In Fig. 10, the  $H$  field is plotted along the  $z$  axis. The difference between FEA and analytical calculation is inferior to 1%.

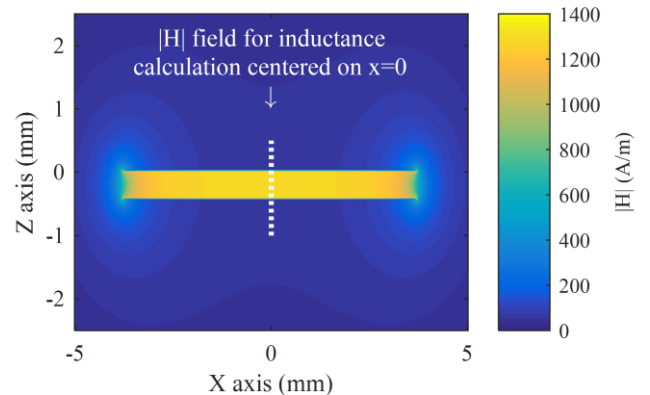


Fig. 8. Analytical result for the  $H$  field computed with (8) and (10). The dimensions are  $e = 0.42$  mm,  $w = 7.5$  mm,  $h = 35$   $\mu$ m,  $I = 10$  A.

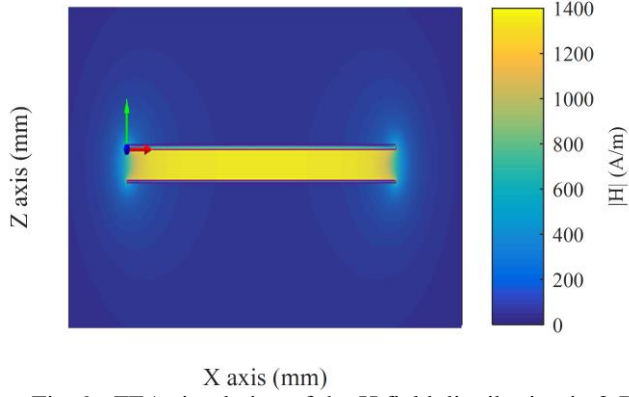


Fig. 9. FEA simulation of the H field distribution in 2-D with Magnet®. The dimensions are  $e = 0.42$  mm,  $w = 7.5$  mm,  $h = 35$   $\mu$ m,  $I = 10$  A.

When  $w \gg e$ , the curve obtained in Fig. 10 can be approximated by an external  $H$  field of 0 and an internal one of  $I/w$ , which is the basis for the conventional inductance expression of (1).

Within the cope of this paper, our aim is to obtain better accuracy on the PCB inductance value, which will be useful in the accurate estimation of the overvoltage on a transistor at turn-off. To determine the inductance, the flux  $\phi$  between the two

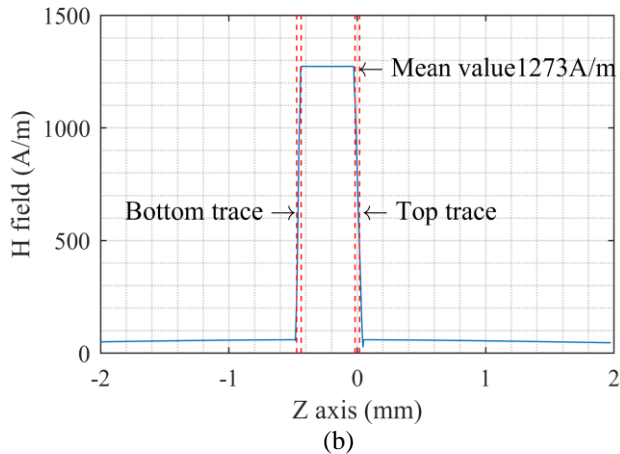
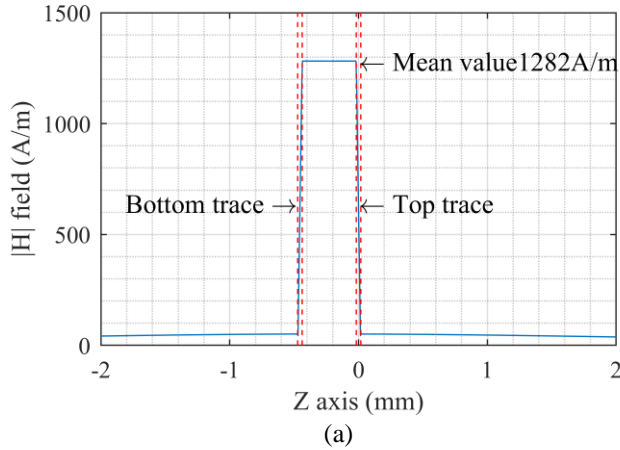


Fig. 10. H comparison between (a) analytical and (b) FEA calculation along the  $z$  axis (for  $x=0$ ). The dimensions are  $e = 0.42$  mm,  $w = 7.5$  mm,  $h = 35$   $\mu$ m,  $I = 10$  A.

plates must be calculated. This is done by integrating the magnetic field over a surface  $S$  parallel to the plane ( $y, z$ ) inside the loop formed by the top layer, bottom layer and the two slots shown Fig. 6.

The flux can be expressed by (11):

$$\phi = \iint_S B_x dS = \mu_0 I \int_{-h/2-e}^{-h/2} [H_{upperX}(0, z_0) + H_{lowerX}(0, z_0)] dz_0 \quad (11)$$

Inserting (11) into (3) gives (12):

$$L_{pcb} = \frac{\mu_0 I}{I} \int_{-h/2-e}^{-h/2} [H_{upperX}(0, z_0) + H_{lowerX}(0, z_0)] dz_0 \quad (12)$$

Then the exact value of the inductance is obtained for the two conductors perfectly aligned, with the same dimensions by inserting (8) and (10) into (12), giving (13). The detail of the inductance calculation is included in the Appendix.

$$\begin{aligned} L_{pcb} = & \frac{\mu_0 I}{\pi w h} \left[ \pi h e + \left( e^2 - \left( \frac{w}{2} \right)^2 \right) \tan^{-1} \left( \frac{2}{w} e \right) \right. \\ & + \left( h^2 - \left( \frac{w}{2} \right)^2 \right) \tan^{-1} \left( \frac{2}{w} h \right) - \left( (e+h)^2 - \left( \frac{w}{2} \right)^2 \right) \tan^{-1} \left( \frac{2}{w} (e+h) \right) \\ & \left. + \frac{w}{2} \left( e \log \left( \frac{(e+h)^2 + \left( \frac{w}{2} \right)^2}{e^2 + \left( \frac{w}{2} \right)^2} \right) + h \log \left( \frac{(e+h)^2 + \left( \frac{w}{2} \right)^2}{h^2 + \left( \frac{w}{2} \right)^2} \right) \right) \right] \quad (13) \end{aligned}$$

Of course, the resulting inductance expression is a bit cumbersome compared to the conventional (1). This issue is addressed in the next section, with a more usable approximation, and where accuracy is enhanced compared to (1).

#### IV. FORMULA SIMPLIFICATION

##### A. Standard approximation limits

For small track width  $w$ , the  $H$  field along the  $z$  axis is displayed in Fig. 11 (for  $w/e = 1$  and  $h = 35$   $\mu$ m). The mean value of  $|H|$  calculated with (8) and (10) between the two traces is 12183 A/m while the traditional approximation using  $I/w$  will give 23810 A/m, with an error of 95% on the field estimated and inductance calculation.

In the application where GaN transistors are used with the loop and dimensions highlighted in Fig. 6, the width is close to the space between the conductors, (1) cannot be used. Fig. 12 shows the difference in inductance value calculated with (13) compared to the value obtained with (1) for typical GaN transistors footprint. Differences over 10% are obtained. The conductor width associated to some GaN components and the driver loop size are also indicated on Fig. 12. As presented in Fig. 12, even if the approximation is suitable for wide copper traces, it is not suited for the fast switching GaN technology. A new estimation formula with a lower error and higher range of use is then needed.



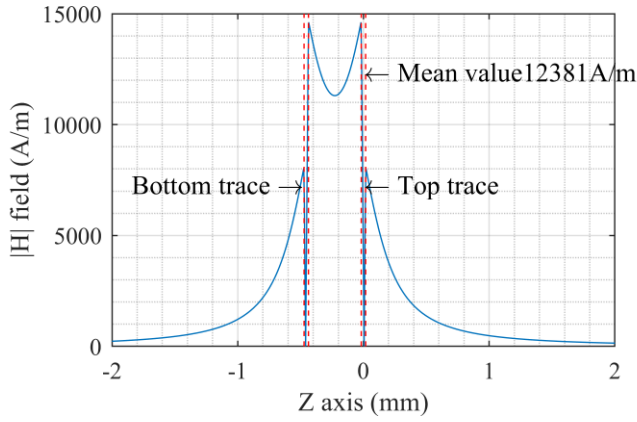


Fig. 11.  $|H|$  along the  $z$  axis, for  $x = 0$  with a reduced size of  $w = 0.42$  mm and  $e = 0.42$  mm, the traditional approximation cannot be used in this case.

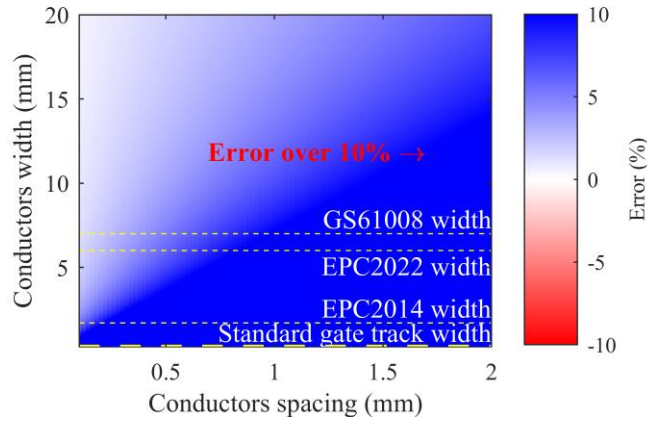


Fig. 12. Difference between  $L_{pcb}/l$  calculated with (1) and  $L_{pcb}/l$  calculated with (13). The error becomes significantly higher than 10% for a ratio of  $w/e < 7$ . The indicated GaN components width shows that their inductance cannot be well estimated with (1). EPC2022, EPC2014 and GS61008 are GaN transistors available on the market.

### B. Proposed Approximation

To overcome this limitation, (13) can be approximated with (14), using the assumption that  $50 \text{ mm} > w > 0.25 \text{ mm}$  and  $2 \text{ mm} > e > 100 \mu\text{m}$ . The approximation was conducted using curve fitting numerical tools. The inductance per meter  $L_{pcb}/l$  was first calculated for the previously given dimensions, considering the standard value of  $h = 35 \mu\text{m}$ . Then, using (1) as a starting point, the custom equation (14) coefficients were found thanks to the least square algorithm of Levenberg-Marquardt [8].

$$L_{pcb} \cong \mu_0 \frac{e}{w} l \left( \frac{1}{1 + e/w} + 0.024 \right) \quad (14)$$

The resulting approximation shows a  $R^2$  coefficient of 0.999, indicating an extremely close result between the exact formula and the estimation considering that a  $R^2$  of 1 is a perfect approximation. (14) introduces a correction factor to the conventional expression (1) with the term within parentheses with a maximum error of 6% observed in the studied range. Fig. 13. shows the difference between (14) and (13), the ranges for

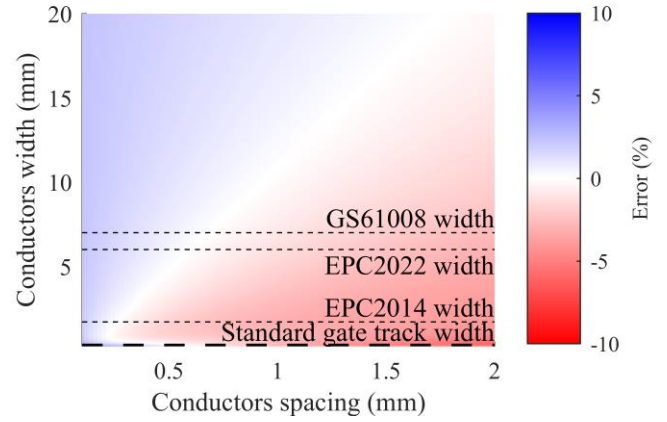


Fig. 13. Difference between  $L_{pcb}/l$  calculated with (14) and  $L_{pcb}/l$  calculated with (13). The error is limited to 6%. The indicated GaN components width shows that their inductance can be well estimated with (14).

the loop width  $w$  and spacing  $e$  are adapted to allow the dimensions of different GaN components to be seen. The result is greatly improved, and the resulting formula remains easy to use. With this new approximation, the power loop inductance and the gate loop inductance can be found with a known maximal error allowing to evaluate the loop characteristics at the design stage.

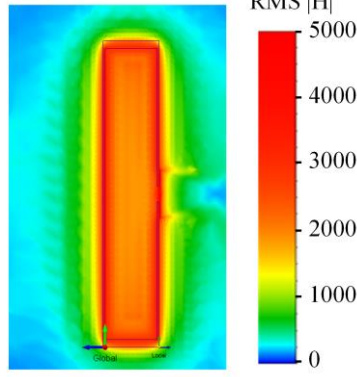
The comparison is conducted for the power loop of components EPC2014, GS61008 and also to calculate the gate-source driver loop. The result in Table 1 shows that the new proposed equation allows for a better estimation of the inductance for various size of tracks. In particular, for the gate-source stray inductance, it becomes possible to estimate standard (0.254 mm) tracks inductance. The error is reduced from more than 300% with (1) to less than 4% with (14). The deviation between the FEA 3D simulation and the approximated value of (14) is within 10%. A similar comparison is made with the top-bottom loop topology detailed in II.B. The result is given Fig. 14. The flux is well concentrated between the conductors, (1), (13) and (14) can then be applied to this topology and the result is given in the table inside Fig. 14.

Table 1. Comparison between the FEA result and the analytical formulas for different GaN HEMT components, power loop and driver loop.

Component	EPC2014 power loop	GS61008 power loop	EPC2014 Gate drive loop
Loop dimensions ( $w \times l \times e$ ) (mm)	1.7 x 9.5 x 1	7 x 15.5 x 1	0.254 x 7.2 x 1
$L_{pcb}$ with (13) (exact expression)	4.67 nH	2.52 nH	7.82 nH
$L_{pcb}$ with (14) (new approximation), error	4.60 nH, 1.5%	2.50 nH, 0.8%	8.11 nH, 3.7%
$L_{pcb}$ with (1) (classical approximation), error	7.02 nH, 50%	2.78 nH, 10%	35.6 nH, 355%
$L_{pcb}$ FEA result with Magnet®_error	4.31 nH, 7.7 %	2.28 nH, 9.5%	8.81 nH, 13%



Top-Bottom topology H field  
side view for the EPC2014 dimensions



(a)

Component	EPC2014
Loop dimensions ( $w, l, e$ )	1.7 mm x 9.5 mm x 1.6 mm
FEA result with Magnet®	5.72 nH
Result of (1) and error	11.2 nH, 96%
Result of (13) and error	6.20 nH, 8.4%
Result of (14) and error	6.07 nH, 6.1%

(b)

Fig. 14. Simulation of the Top-Bottom for the component EPC2014, (a) the FEA simulation result, (b) inductance result and calculation for this topology.

It appears that the proposed formula (14) allows estimation better estimation (6.1 % difference with FEA) if compared to the classical approximation (1), which exhibits an error of 96%. It shows the adequacy of the proposed solution to two geometries (internal layer and Top-Bottom).

## V. PRACTICAL VALIDATION

To validate both the analytical expression (13) of  $L_{pcb}$  and the approximated (14), a laboratory test is conducted, using a GaN HEMT with the prototype visible Fig. 15. Each important part is shown and the inductances that appear are calculated with (14). This prototype allowed for validation of the numerical approach and to perform power measurement. The dimensions and the small  $e$  value of 175μm have been chosen to allow the smallest inductance, hence the smallest overshoot possible. This prototype can switch currents on a ns scale and thus needs a very low inductance in its power loop. We use a 1 mm-thick PCB with 2 internal layers ( $e = 175 \mu\text{m}$ ). The component used is the GS61008p from GaNSystems ( $w = 7 \text{ mm}$ ). The power path architecture uses the optimized topology presented in Fig. 6.

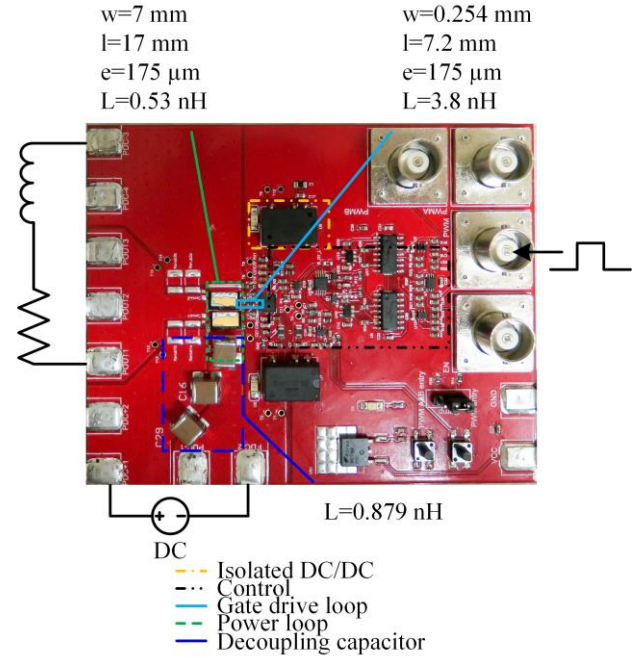


Fig. 15. Simulation of the Top-Bottom for the component EPC2014, (a) the FEA simulation result, (b) inductance result and calculation for this topology.

When switching the result of the low side rising voltage is the one presented in Fig. 16.

A common way to measure the stray loop inductance is to measure the ringing frequency using (15).

$$L_{stray} = \frac{1}{C_{oss} (2\pi f_{ring})^2} \quad (15)$$

The PCB loop inductance is then obtained by subtracting the two inductances of the transistor package  $L_{Q1}$  and  $L_{Q2}$ . Using the component technical document,  $C_{oss}(50 \text{ V}) = 280 \text{ pF}$ . Then the measured inductance is  $L_{stray} = 1.45 \text{ nH}$ . Considering a package inductance of 0.1 nH per transistor, similar to the one given by the HEMT manufacturer EPC [13], and removing the capacitors total inductance of 0.87 nH we can deduce the

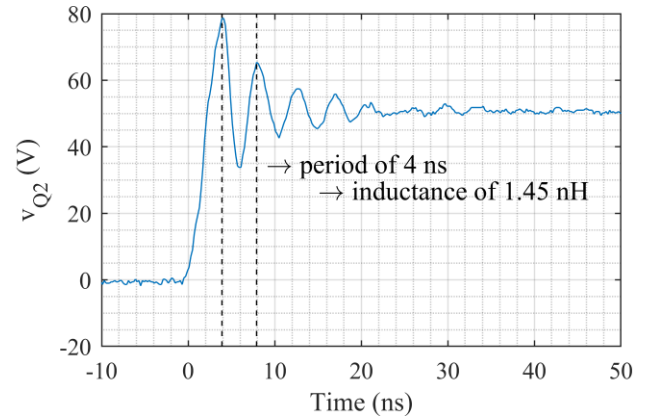


Fig. 16. Low side turn-off voltage, an overvoltage and ringing occur, due to the PCB power path inductance and the internal component capacitance  $C_{oss}$

experimental value of the PCB loop inductance to be  $L_{pcb(measured)} = 0.38$  nH.

Using (14), the approximated theoretical value is 0.53 nH, giving a difference of 150 pH between measurement and theory. The obtained error comes from the lack of detailed packaging inductance analysis from the manufacturer and some 3-D effects, which are not considered in the field calculation.

Fig. 17 shows the result of the obtained inductance depending on the  $e/w$  ratio. It appears clear that the traditional approximation introduces a high error with a ratio over 0.2. The gate loop values taken for the graph are the ones calculated with the FEA method and shows a very close match with the presented work, while the traditional calculation exhibits a very high error.

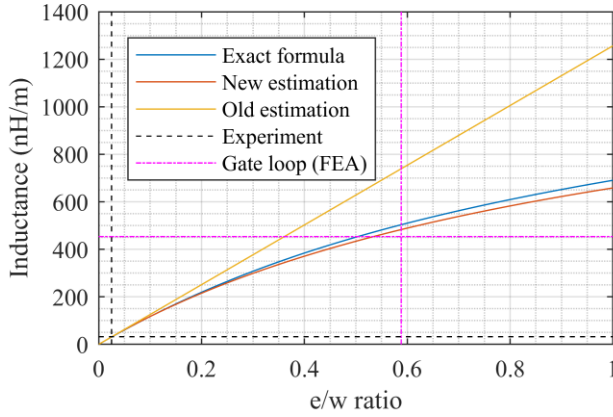


Fig. 17.  $e/w$  ratio and the location of the experiment and a gate loop inductance calculation

## VI. CONCLUSION

This paper presented the most optimized power loop for high speed switching devices like GaN power transistors. Many studies use this topology and the value of the PCB inductance is known through PCB numerical simulation or formula approximation. These two tools have advantages and drawbacks, such as time consumption or unknown error. The paper presented a complete 2-D analysis of the magnetic field obtained between two conducting plates, by using Biot-Savart law and allowed to demonstrate that the conventional inductance formulation is an approximation that can no longer be used in certain form factors, especially with small conductors. It was found that for PCB traces of width/spacing inferior to 7, traditional expression (1) will overestimate the inductance by more than 10%. With a ratio of 1, this overestimation increases to 95%.

To improve the inductance estimation, a new formula is proposed by (14). It remains easy to use and was tested for numerous width and conductor spacing with a FEA software. The validation through a practical experience shows the correspondence between the real measurement and the new approximation. This work intends to help the design of high speed switching loops where all the stray inductances need to be known at the design stage of the power converters.

## APPENDIX I

The detailed calculation steps to solve (4) and obtain  $H_{upper}$  and  $H_{lower}$  are presented here. The  $H$  field calculated is only for one conductor, to obtain the total field at each point, the solutions of both the top and the inner conductors must be added.

$$\begin{cases} H_{upperX}(x_0, z_0) = \frac{J}{2\pi} \int_{-w/2}^{w/2} \int_{-h/2}^{h/2} \frac{z_0 - z}{(z_0 - z)^2 + (x_0 - x)^2} dz dx \\ H_{upperY}(x_0, z_0) = 0 \\ H_{upperZ}(x_0, z_0) = -\frac{J}{2\pi} \int_{-h/2}^{h/2} \int_{-w/2}^{w/2} \frac{x_0 - x}{(z_0 - z)^2 + (x_0 - x)^2} dx dz \end{cases} \quad (16)$$

Knowing that

$$\ln(u)' = \frac{u'}{u} \quad (17)$$

$$\begin{cases} H_{upperX}(x_0, z_0) = -\frac{J}{4\pi} \int_{-w/2}^{w/2} \int_{-h/2}^{h/2} \left[ \ln((z_0 - z)^2 + (x_0 - x)^2) \right] dx \\ H_{upperZ}(x_0, z_0) = -\frac{J}{4\pi} \int_{-h/2}^{h/2} \int_{-w/2}^{w/2} \left[ \ln((z_0 - z)^2 + (x_0 - x)^2) \right] dz \end{cases} \quad (18)$$

$$\begin{cases} H_{upperX}(x_0, z_0) = \frac{J}{4\pi} \int_{-w/2}^{w/2} \ln(4(x - x_0)^2 + (h + 2z_0)^2) \\ \quad - \ln(4(x - x_0)^2 + (h - 2z_0)^2) dx \\ H_{upperZ}(x_0, z_0) = \frac{J}{4\pi} \int_{-h/2}^{h/2} \ln(4(z - z_0)^2 + (w + 2x_0)^2) \\ \quad - \ln(4(z - z_0)^2 + (w - 2x_0)^2) dz \end{cases} \quad (19)$$

To calculate the complete integral, solving the following equation is needed.

$$\int \ln(c(x+a)^2 + b) dx \quad (20)$$

$$\begin{aligned} & \int \ln(c(x+a)^2 + b) dx \\ &= (a+x) \ln(c(x+a)^2 + b) - 2 \int \frac{c(x+a)}{c(x+a)^2 + b} dx \end{aligned} \quad (21)$$

$$\begin{aligned} & \int \ln(c(x+a)^2 + b) dx \\ &= (a+x) \ln(c(x+a)^2 + b) - 2 \int dx + 2 \int \frac{1}{\frac{c(x+a)^2}{b} + 1} dx \end{aligned} \quad (22)$$

$$\begin{aligned} & \int \ln(c(x+a)^2 + b) dx \\ &= \left[ (a+x) \ln(c(x+a)^2 + b) - 2x + 2\sqrt{\frac{b}{c}} \tan^{-1} \left( \sqrt{\frac{c}{b}} (a+x) \right) \right] \end{aligned} \quad (23)$$

Applied to  $H_x$  with  $a = -x_0$ ,  $b = (h + 2z_0)^2$ ,  $c = 4$  for the first logarithm term and  $a = -x_0$ ,  $b = (h - 2z_0)^2$ ,  $c = 4$  for the second logarithm term, it comes:

$$H_{upperX}(x_0, z_0) = \frac{J}{4\pi} \left[ (x - x_0) \ln \left( \frac{4(x - x_0)^2 + (h + 2z_0)^2}{4(x - x_0)^2 + (h - 2z_0)^2} \right) + (h + 2z_0) \tan^{-1} \left( \frac{2(x - x_0)}{h + 2z_0} \right) - (h - 2z_0) \tan^{-1} \left( \frac{2(x - x_0)}{h - 2z_0} \right) \right]_{-w/2}^{w/2} \quad (24)$$

$$H_{upperX}(x_0, z_0) = \frac{J}{8\pi} \left[ 2 \cdot (2z_0 - h) \tan^{-1} \left( \frac{2w(h - 2z_0)}{(h - 2z_0)^2 - w^2 + 4x_0^2} \right) + 2 \cdot (2z_0 + h) \tan^{-1} \left( \frac{2w(h + 2z_0)}{(h + 2z_0)^2 - w^2 + 4x_0^2} \right) \right. \\ \left. - (w - 2x_0) \ln \left( \frac{(w - 2x_0)^2 + (h - 2z_0)^2}{(w - 2x_0)^2 + (h + 2z_0)^2} \right) - (w + 2x_0) \ln \left( \frac{(w + 2x_0)^2 + (h - 2z_0)^2}{(w + 2x_0)^2 + (h + 2z_0)^2} \right) \right] \quad (25)$$

By applying the same methodology to  $H_{upperZ}$ , it comes:

$$H_{upperZ}(x_0, z_0) = \frac{J}{8\pi} \left[ 2 \cdot (2x_0 - w) \tan^{-1} \left( \frac{2h(w - 2x_0)}{(w - 2x_0)^2 - h^2 + 4z_0^2} \right) + 2 \cdot (2x_0 + w) \tan^{-1} \left( \frac{2h(w + 2x_0)}{(w + 2x_0)^2 - h^2 + 4z_0^2} \right) \right. \\ \left. - (h - 2z_0) \ln \left( \frac{(w - 2x_0)^2 + (h - 2z_0)^2}{(w + 2x_0)^2 + (h - 2z_0)^2} \right) - (h + 2z_0) \ln \left( \frac{(w - 2x_0)^2 + (h + 2z_0)^2}{(w + 2x_0)^2 + (h + 2z_0)^2} \right) \right] \quad (26)$$

Then, the final field, including both conductors of the same dimensions with a spacing of  $e$  is:

$$H_x(x_0, z_0) = \frac{J}{8\pi} \left[ -2(h - 2z_0) \left( \tan^{-1} \left( \frac{2w(h - 2z_0)}{(h - 2z_0)^2 - w^2 + 4x_0^2} \right) + 2(h + 2z_0) \tan^{-1} \left( \frac{2w(h + 2z_0)}{(h + 2z_0)^2 - w^2 + 4x_0^2} \right) \right. \right. \\ \left. \left. + 2(2e + h + 2z_0) \tan^{-1} \left( \frac{2w(2e + h + 2z_0)}{(2e + h + 2z_0)^2 - w^2 + 4x_0^2} \right) - 2(2e + 3h + 2z_0) \tan^{-1} \left( \frac{2w(2e + 3h + 2z_0)}{(2e + 3h + 2z_0)^2 - w^2 + 4x_0^2} \right) \right. \right. \\ \left. \left. + (w - 2x_0) \ln \left( \frac{((w - 2x_0)^2 + (2e + h + 2z_0)^2)((w - 2x_0)^2 + (h + 2z_0)^2)}{((w - 2x_0)^2 + (2e + 3h + 2z_0)^2)((w - 2x_0)^2 + (h - 2z_0)^2)} \right) \right. \right. \\ \left. \left. + (w + 2x_0) \ln \left( \frac{((w + 2x_0)^2 + (2e + h + 2z_0)^2)((w + 2x_0)^2 + (h + 2z_0)^2)}{((w + 2x_0)^2 + (2e + 3h + 2z_0)^2)((w + 2x_0)^2 + (h - 2z_0)^2)} \right) \right] \quad (27)$$

$$H_z(x_0, z_0) = \frac{J}{8\pi} \left[ -2(w - 2x_0) \left( \tan^{-1} \left( \frac{2w(h - 2z_0)}{(h - 2z_0)^2 - w^2 + 4x_0^2} \right) + \tan^{-1} \left( \frac{2h(w - 2x_0)}{(w - 2x_0)^2 + (3h + 2(z_0 + e))(h + 2(z_0 + e))} \right) \right) \right. \\ \left. + 2(w + 2x_0) \left( \tan^{-1} \left( \frac{2h(w + 2x_0)}{(w + 2x_0)^2 - h^2 + 4z_0^2} \right) + \tan^{-1} \left( \frac{2h(w + 2x_0)}{(w + 2x_0)^2 - (3h + 2(z_0 + e))(h + 2(z_0 + e))} \right) \right) \right. \\ \left. - (h - 2z_0) \ln \left( \frac{(w - 2x_0)^2 + (h - 2z_0)^2}{(w + 2x_0)^2 + (h - 2z_0)^2} \right) - (h + 2z_0) \ln \left( \frac{(w - 2x_0)^2 + (h + 2z_0)^2}{(w + 2x_0)^2 + (h + 2z_0)^2} \right) \right. \\ \left. - (h + 2e + 2z_0) \ln \left( \frac{(w - 2x_0)^2 + (2e + h + 2z_0)^2}{(w + 2x_0)^2 + (2e + h + 2z_0)^2} \right) + (3h + 2ew + 2z_0) \ln \left( \frac{(w - 2x_0)^2 + (2e + 3h + 2z_0)^2}{(w + 2x_0)^2 + (2e + 3h + 2z_0)^2} \right) \right]$$

To calculate the inductance, the flux between the two plates must be calculated. The surface is considered parallel to the plane (y, z) and inside the loop formed by the top layer, bottom layer and the two slots as shown Fig. 6.

$$\varphi_B = \iint_S \mu H \cdot dS = \mu l \int_{-h/2-e}^{-h/2} H_x(0, z_0) dz_0 \quad (28)$$

$$L_{PCB} = \frac{\mu l}{I} \int_{\frac{h}{2}-e}^{-\frac{h}{2}} [H_x(0, z_0)] dz_0 \quad (29)$$

Then the exact value of the inductance for the two conductors perfectly aligned, with the same dimensions is:

$$L_{pcb} = \frac{\mu_0 l}{\pi w h} \left[ \pi h e + \left( e^2 - \left( \frac{w}{2} \right)^2 \right) \tan^{-1} \left( \frac{2}{w} e \right) + \left( h^2 - \left( \frac{w}{2} \right)^2 \right) \tan^{-1} \left( \frac{2}{w} h \right) - \left( (e+h)^2 - \left( \frac{w}{2} \right)^2 \right) \tan^{-1} \left( \frac{2}{w} (e+h) \right) + \frac{w}{2} \left( e \log \left( \frac{(e+h)^2 + \left( \frac{w}{2} \right)^2}{e^2 + \left( \frac{w}{2} \right)^2} \right) + h \log \left( \frac{(e+h)^2 + \left( \frac{w}{2} \right)^2}{h^2 + \left( \frac{w}{2} \right)^2} \right) \right) \right] \quad (30)$$

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