Overvoltage reduction with enhanced snubber design for GaN-based Electric Vehicle Drive

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***Abstract*—Power electronics applied to electrical vehicle is a field where power density, cost and weight are the main factors for dimensioning a power converter. In this context, one of the trends is to increase the working frequency and use smaller components. This can be achieved with components using technologies that allow an extremely small switching time while keeping the breakdown voltage and current as high as possible. This contemporary trend leads to the use of new materials such as Gallium Nitride or Silicon Carbide. Gan transistors in particular, with switching time as low as 2 ns lead to high overvoltages even with minimized power loop inductances. This overshoot can be addressed by adding an external circuitry known as snubber. While it is widely used, there are difficulties in its modeling and predicting its impact on the transient waveform.**

This paper aims to present the snubber circuitry applied to fast switching components such as GaN transistors. A mathematical model considering the internal parameters of the transistor is proposed. This model will be used to predict the overvoltage and the impact of the snubber. The mathematical approach is tested by simulation, considering an EPC component on a PCB having a loop inductance of 0.7nH and a dv/dt of 25 V/ns. The waveform improvement and losses are compared and the first results show significant improvement in the voltage waveform with lower overvoltage and ringing.

Index Terms—HEMT; Power Electronics; Fast Switching; Modeling; GaN; Wide Band Gap, Design, Snubber, electrical vehicle

I. Introduction

Modern vehicle design trends aim for a lower fuel consumption and a better driving experience. These two requirements can be fulfilled by using an electrical power source in the drive train as illustrated in Fig. 1, which depicts a parallel hybrid drivetrain. Pure Electric Vehicle (EV) also make use of similar power electronics requirements. In any case, the electric power circuitry must be light, small and have high efficiency.

Hard switching three-phase voltage source inverter in combination with adjustable DC-DC front-end converter is a very common approach for modern EV [1] or hybrid and can be found in the Toyota Prius design [2]. To achieve compact converters, short switching times are desirable, implying high di/dt and dv/dt. New semiconductor technologies with wide band gap (WBG) such as Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) enable the desired extremely fast switching times with di/dt in the 50 A/ns range and dv/dt in the 100 V/ns range, leading the way for MHz-switching frequencies. The GaN technology thus has a great potential for high power density improvement [3]. Such fast rise and fall times will impact the overall design, down from the lower power components of the drive-circuit, up to the high-power PCB traces which inductive behavior is not to be neglected. These stray inductances will store a magnetic energy, which in turn will produce an overvoltage and a ringing when turning off the transistors, when hard switching is applied [4] as presented in Fig. 2 with a dv/dt of 25 V/ns where a 92 V overvoltage is observed on a 50 V voltage source. These phenomena can lead to electromagnetic compatibility (EMC) issues [5], overheating

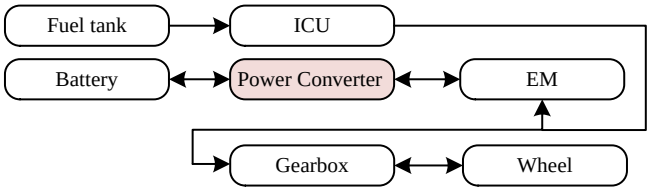


Fig. 1, ICU: internal combustion engine, EM: Electrical motor Simplified hybrid parallel vehicle power train architecture. The overshoot issue is in the power converter.

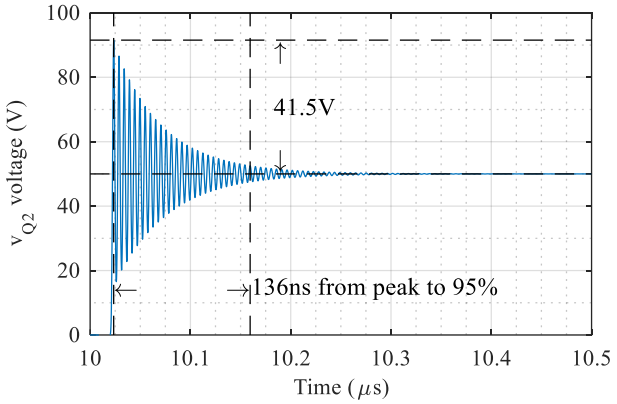


Fig. 2, Spice simulation result for 0 A hard switching with a stray inductance of 0.7 nH, the dv/dt is 25 V/ns. The overshoot is due to the stray inductance resonating with the HEMT internal capacitor.

and component derating. These issues can compromise the gains made by the WBG technology and increase the converter price while lowering its performances. To address this problem, many methods are reported, some use a dedicated gate drive circuit which controls the maximum voltage [6], energy recovery [7] or dissipative snubber [8][9]. Such technologies will use circuit space making it usable or not depending on the circuitry size. More important, these methods refer to Si-MOSFET based power electronics, which compatibility with ns-range switching of GaN HEMT is yet to be demonstrated. The envisioned High Electron Mobility Transistor (HEMT), based on GaN technology, is very small and very little space allowed to external circuitry is a valuable feature. A simple and small circuit adapted to our case is the typical RC snubber, which usefulness in the case of GaN half-bridge HEMT will be discussed in this paper. While this approach is widely known in many applications, very few papers [10] provide the explanation on the dimensioning of this kind of circuit using analytical expressions, especially needed in the case of GaN HEMT switching.

II. SNUBBER TOPOLOGIES

A. *Energy recovery snubber*

Energy recovery snubbers intend to limit the overvoltage due to the hard switching while keeping the efficiency as high as possible. To do so, these snubbers recover the energy accumulated when limiting the overvoltage. Many topologies exist and present good performances [11],[12]. This approach is mainly used for high-power systems since more space is available and the high losses obtained without recovery would lead to high temperatures rise.

The drawback of the energy recovery snubbers technology resides in the complicated circuitry, which usually includes a number of diodes for which stray inductances may be an issue in the ns-range. Such energy recovery snubbers will use a non-negligible PCB space and are not adapted to very small components like GaN power switching devices in Fig. 3

Fig. 3 Comparison of a D²PAK standard packaging to an EPC EPC2010C, a 100 V, 22 A transistor which is 20 times smaller. (Image source: www.http://epc-co.com).

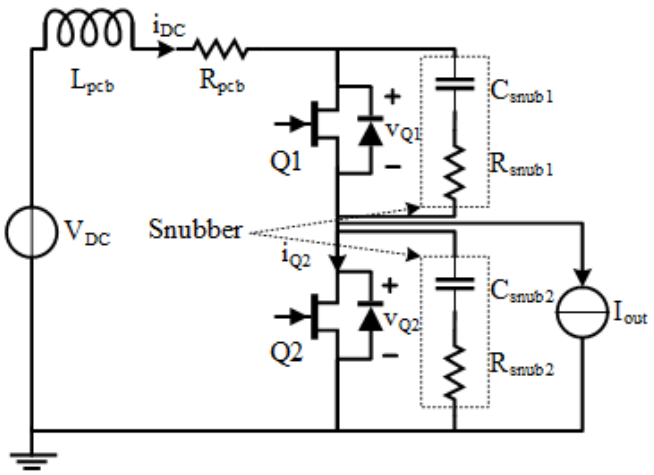


Fig. 4 Switching arm with the PCB inductance and resistance. The output is considered highly inductive and is represented as a DC current load.

showing a comparison between a standard D2PAK Mosfet and 20 times smaller HEMT.

B. *Dissipative snubber*

Dissipative snubbers have the same purpose as the energy recovery snubber. The main difference is that the overshoot energy will be dissipated through the snubber and the transistor. The main topologies are RC and RCD snubbers [13],[14]. Although this may appear as a consequential drawback, it must be pointed out that the amount of energy to be dissipated in the GaN HEMT with their very low intrinsic capacitance C_{oss} is very small, while the positive effect of adding an RC snubber will bring substantial advantage on the overvoltage reduction. The structure studied in the present paper is detailed in Fig. 4, which exhibits a half-bridge of HEMT transistors, the PCB parasitic elements and RC snubbers added in parallel with each of the two transistors. In ns-range GaN circuits, the parasitic PCB inductance has a very significant effect, which needs to be considered in the overall circuit investigation. The circuitry is very simple, in our case, a capacitor in series with a resistor. But obtaining the optimal values of these passive components is non-trivial. On the existing methodologies, the more popular one uses a primary test with an initial set of RC values to find better adapted values [15]. This method requires multiple tests to gather all the data and several modifications or improvements of the PCB are needed. While it can be acceptable for some designs where rework is easily done, the components need to be under rated to withstand the first tuning test.

With the modern numerical tools, it is now possible to predict the value of the PCB traces inductance L_{PCB} based on the geometrical design. Taking this parameter and the transistor properties into account, it is possible to derive an analytical model of the snubber. This work gives a complete waveform calculation based on Fig. 4. This calculation will be able to give the transistor voltage waveform without any primary tests, using only the PCB and transistor characteristics with the values set for the snubber.

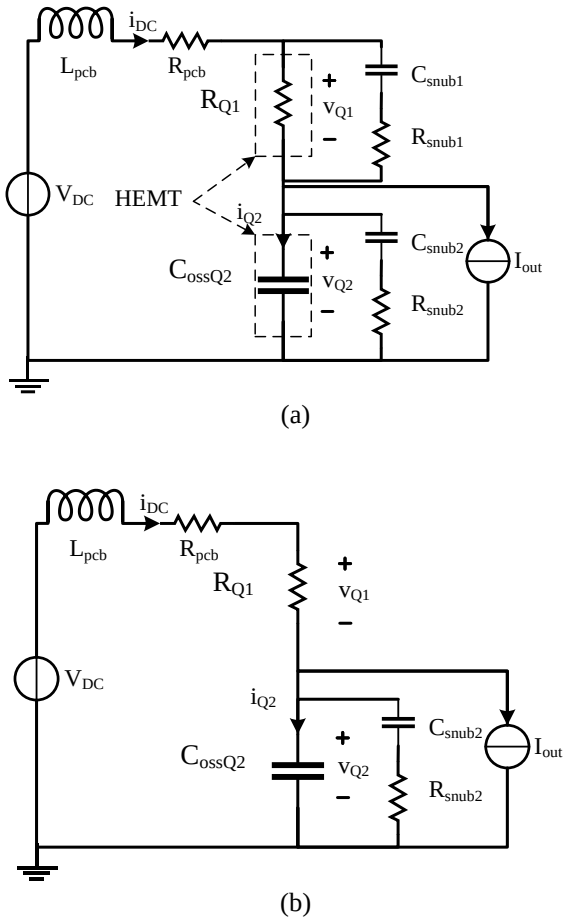


Fig. 5, Model simplification (a) HEMT modeling with the high side conducting and the low side opened. (b) Final model with the high side snubber ignored, due to the v_{Q1} near-constant low voltage.

III. Detailed Calculation of the RC Snubber

A. Modeling method

The focus is set on understanding the impact of the HEMT and PCB properties and their role in the snubber dimensioning. The modeling method is based on Laplace transformation and the use of the switch internal parameters. For the analysis of the circuit behavior when the low-side HEMT turns off, we make the following simplification: we chose to work in complementary mode, where the low-side switch model instantly changes from a full-conduction state to an open state, modeled with a C_{ossQ2} capacitor. At the exact same time, the high-side switch Q1 is closed, instantly changing from a fully blocked condition to a resistance R_{Q1}. Although this assumption is a simplification of the complete switching process, we will show that it enables modeling the snubber-HEMT behavior in an accurate and workable fashion.

The internal resistance R_{Q1} of the high-side HEMT has a very low value and the resulting high-side impedance of R_{Q1} in parallel with the RC snubber can be simplified by considering the internal resistance of the switch only, as shown in Fig. 5 (b), which shows the final model used in (1) for the mathematical model.

Eq. (1) gives the low-side transistor switching waveform v_{Q2} at turn-off, considering the PCB and the transistor parameters. Eq. (1) was derived using conventional circuit analysis. The result is a third order transfer function that needs to be analyzed to find the adapted RC values to reduce the oscillations dynamics of the transient voltage. Naturally, a third order expression was expected, as the circuit contains 3 energy absorption components L_{pcb}, C_{snub2} and C_{ossQ2}.

$$\frac{v_{Q2}}{v_{DC}} = \frac{\tau_{sn}s+1}{\frac{\tau_{sn}}{\omega_0^2}s^3 + \left[\tau_{sn}C_{ossQ2}\left(R_{pcb}+R_{Q1}\right)+\frac{1}{\omega_T^2}\right]s^2 + \left[\tau_{sn}+\tau_T\right]s+1} \quad (1)$$

Where:

$$\tau_{sn} = R_{snub2}C_{snub2} \quad (2)$$

$$\omega_0 = \frac{1}{\sqrt{L_{pcb}C_{ossQ2}}} \quad (3)$$

$$\tau_T = \left(R_{pcb}+R_{Q1}\right)\left(C_{ossQ2}+C_{snub2}\right) \quad (4)$$

$$\omega_T = \frac{1}{\sqrt{L_{pcb}\left(C_{ossQ2}+C_{snub2}\right)}} \quad (5)$$

From this point, it is not possible to clearly express (1) into the product of a first-order system and a second-order system, which would allow to easily extract a clear damping factor. The analysis needs to be conducted on the whole expression. The first step is to validate the derived expression (1) by comparing with the Spice simulation waveform, which is presented in Fig. 2. As the model already represents the switches final state with Q1 as a resistance and Q2 as a capacitor, v_{DC} is used to generate the voltage step corresponding to the switching transient. In the real implemented circuit, V_{DC} is continuous and the voltage across Q1 will drop. These two voltages are in series, i.e. a sum of two voltages. Here, we make the choice to assume that v_{DC} *(s)* will behave as a step at the same time where the switch models operate a change as in Fig. 6.

This is done with a v_{DC} voltage input being a step with a slope corresponding to a rise time of 1.6 ns, per the component properties and the gate drive simulated. The result is presented in Fig. 7.

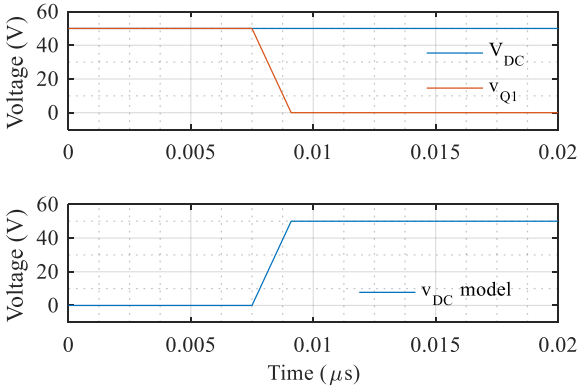


Fig. 6, Combination of the practical waveforms and the v_{DC} used for the waveform calculations.

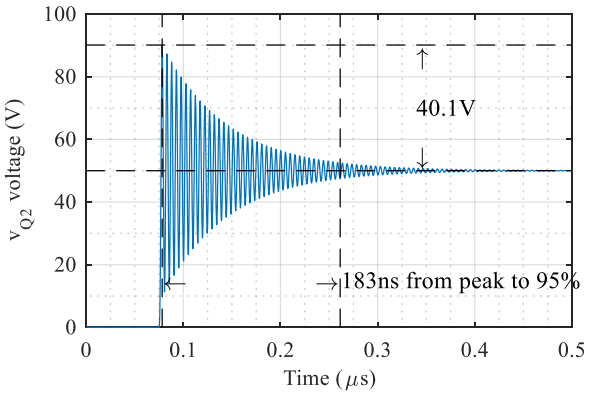


Fig. 7, Result of (1) simulated with Matlab©, using the same parameters as the Spice simulation presented in Fig. 2. R_{snub2} = 10 MΩ, C_{snub2} = 0.01 pF

The values of C_{ossQ2} and L_{pcb} used are 850pF and 700 pH respectively. R_{snub2} is set to an extremely high value of 10MΩ to emulate the «snubberless» circuit behavior for comparison, giving a high τ_{sn}. In the Spice simulation of Fig. 2, a time duration between peak and steady-state value ±5% of 136 ns, a peak value of 91.5 V and an oscillation frequency f_0 of 191MHz have been observed. For the same parameters, (1) gives a stabilization time of 183 ns, a peak value of 90.1 V and an oscillation frequency of 191 MHz as seen in Fig 6. The small difference can be explained by many factors, one being the HEMT parameters graphical reading.

The error in the value of the peak voltage is limited to less than 2% of the peak value. Many factors can help in explaining this difference. The parameters for the analytical calculation are taken from the component technical document and the reading on the curves can introduce a limited error.

Another important factor is the use in (1) of a linear system to model the switching behavior, whereas in the Spice simulation and in reality, C_{ossQ2} adopts a non-linear behavior, and varies with the component voltage.

Thus, the reported error is lower than 2%, which indicates very good potential for the prediction of the v_{Q2} waveform at turn-off, the latter will be used to predict the snubber influence.

IV. Transfer Function Analysis and Snubber Design

The transfer function (1) may be difficult to analyze as is. To conduct a proper study, (1) is analyzed as if it was the combination of an open-loop transfer function *G(s)* with a feedback transfer function *H(s)* connected in a closed loop form, as presented in Fig. 9. This process will allow to obtain a workable form for *G(s)*, from which the phase margin and gain margin methodology can further be used to optimize the transient response, as would be done in the case of a closed-loop system. In turn, the selection of the R_{snub} and C_{snub} values will allow to obtain a suitable value based on the selected snubber losses to maximize the phase margin. As is well known, increasing the Phase Margin on the open-loop response will decrease the oscillatory behavior of the closed-loop response. By analyzing the closed loop transfer function (6) we can obtain *G(s)* and *H(s)*, given by (7) and (8).

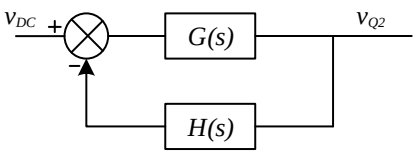


Fig. 9, Closed loop considered for the analysis of (1)

It can be shown that (1) is equal to (6):

$$\frac{v_{Q2}}{v_{DC}} = \frac{G(s)}{1+G(s)H(s)} \tag{6}$$

where

$$G(s) = \frac{\tau_{sn}s+1}{s^2\left(\frac{\tau_{sn}}{\omega_0^2}s + \tau_{sn}C_{ossQ2}\left(R_{pcb}+R_{Q1}\right)+\frac{1}{\omega_T^2}\right)} \tag{7}$$

and

$$H(s) = \frac{\left(\tau_{sn}+\tau_T\right)s+1}{\tau_{sn}+1} \tag{8}$$

Now these expressions allow for open loop analysis performed on the product of *G(s).H(s)*. The analysis without the snubber can be conducted by choosing an extremely high value of R_{snub2} or a value of 0 for C_{snub2}. The result for the open loop in the "snubberless" case is presented in Fig. 8 where we can observe a phase margin (PM) of only 1.3° explaining the high overshoot in the "snubberless" response of Fig. 7.

Finding the optimal value for R_{snub2} is of high importance to obtain the lowest overshoot with a defined C_{snub2}. To find the optimum snubber resistor, its impact on the phase margin needs to be studied by solving (9). The solution is (10), allowing for a systematic design.

$$\frac{\partial Arg\left(G(s)H(s)\right)}{\partial R_{snub}} = 0 \tag{9}$$

$$R_{snub} = \frac{\omega_0^2\omega^2\omega_T}{C_{sn}\left(C_{Q2}^2R_{tot}^2\omega_0^4\omega_T^2+\omega^2\left(\omega_T^2-\omega_0^2\right)\right)}\left[\left(\tau_T - C_{Q2}R_{tot}\frac{\omega_0^2}{\omega^2}\right)\right.$$
$$\left.-\sqrt{\frac{1}{\omega_0^2}\left(\tau_T^2+\frac{1}{\omega^2}\right)\left(C_{Q2}^2R_{tot}^2\frac{\omega_0^4}{\omega^2}+1\right)-2\frac{1}{\omega^4\omega_T^2}\left(C_{Q2}R_{tot}\tau_T\omega_0^2+1\right)+\frac{\omega_0^2}{\omega_T^4\omega^2}}\right] \tag{10}$$

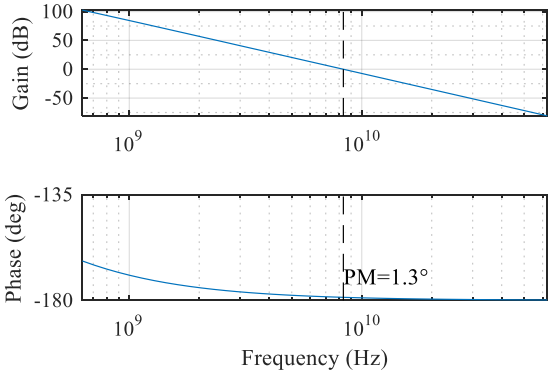


Fig. 8, Bode diagram for the open loop analysis of v_{Q2} response without snubber. The phase margin is very small and explain the high overshoot and ringing.

With

$$R_{tot} = R_{Q1} + R_{pcb} \tag{11}$$

And ω the frequency for which R_{snub} must be optimal, typically the transfer function frequency for 0dB gain.

In this case, a C_{snub2} value of 850 pF (i.e. $C_{snub2} = C_{oss}$) is chosen, which in turns provide an optimal value for R_{snub2} of 1.6 Ω, according to (10). With these values, the open loop diagram is modified as in Fig. 10. The PM is significantly increased to 21°, showing the usefulness of the snubber for stability enhancement. This improves the v_{Q2} voltage damping and will reduce the overshoot value.

Applying a step input to (1) is the worst possible case in term of hard switching and is used to verify the PM improvement in Fig. 10 thanks to the waveform output in Fig. 11. The obtained result shows a great improvement with a ringing lasting only 15 ns and an overvoltage reduced by 19%. The overshoot can be predicted thanks to Fig. 12 and thus the HEMT maximum working voltage is given without the need for a simulation.

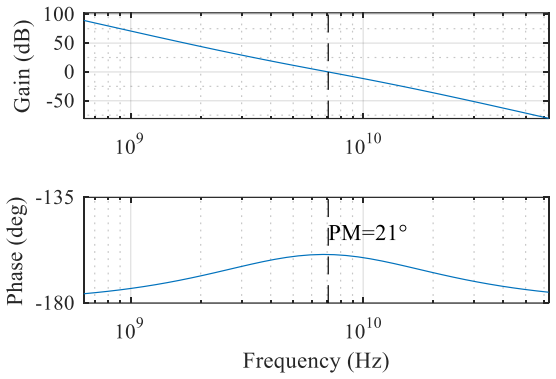


Fig. 10, Bode diagram for the open loop analysis of v_{Q2}. The phase margin is greatly improved thanks to the snubber optimal resistance.

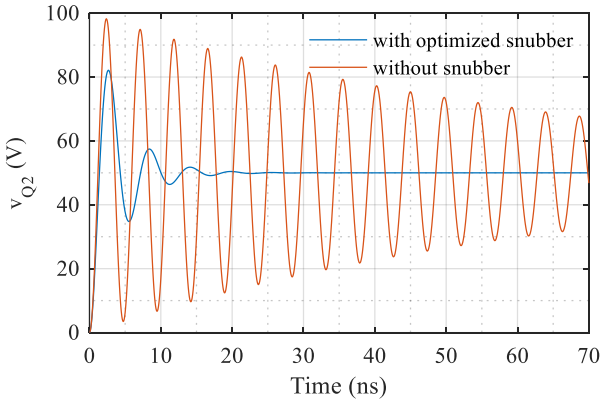


Fig. 11, v_{Q2} response without and with the optimized snubber. The overshoot is greatly reduced and, it is in accordance with the open loop analysis.

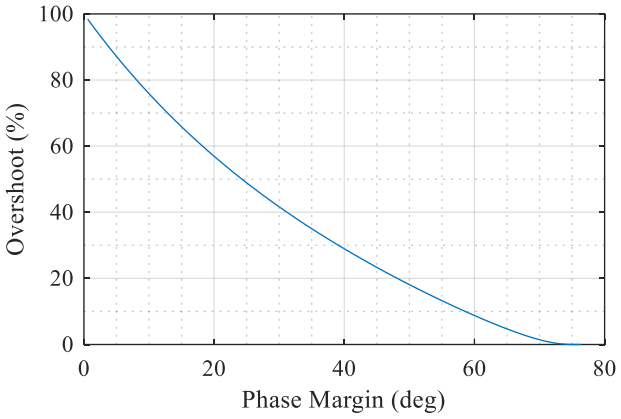


Fig. 12, Overshoot vs phase margin used for closed loop systems.

V. Validation

Using a realistic simulation with Spice, we can see the impact of the PCB parasitic inductor on the v_{Q2} overvoltage as in Fig. 2, the same can be done with the snubber effect. Then a snubber has been added to the HEMT switching device presented Fig. 2. The result is presented in Fig. 13, and shows a greatly improved waveform with a reduced overvoltage from 41.5 V to 28.1 V and a quasi-inexistent ringing. The same snubber parameters have been set in (1) and the result presented in Fig. 14. The mathematical output corresponds to the simulated one with an error as low as 0.3V, validating the snubber improvement and the mathematical expression. For the considered voltage, the losses are 2 W for a 1 MHz switching frequency or 0.2 W for a 100 kHz one. The added losses appear to be very small considering the component current capability of 60 A and the improvement obtained. This makes for a snubber easily designed, thanks to transfer function analyzed through a closed loop methodology. Adding few losses while greatly improving the switching waveform may lead to an overall reduction in the switching losses.

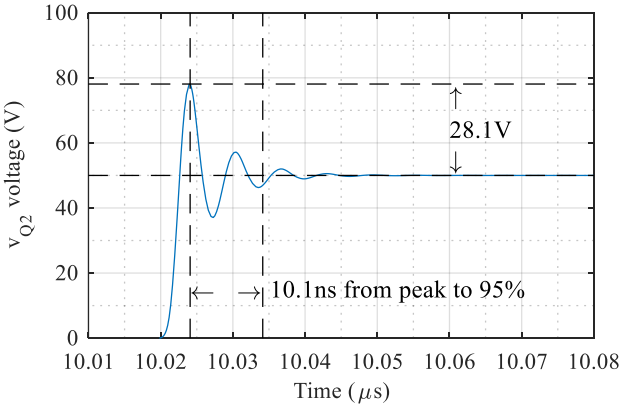
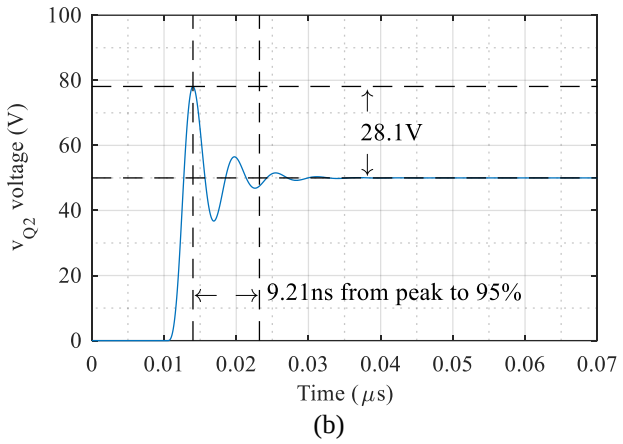


Fig. 13, Spice simulation with a snubber of 850pF and 1.6 Ohm added to the switching HEMT in Fig. 7, the overvoltage has been reduced of 13.4V and the ringing is reduced by 172.2 ns.



(b)

Fig. 14, Result of (1) with the same parameters as in Fig. 13, the error is of 0.3V for the maximal overshoot

VI. Conclusion

This study shows how the RC snubber could be easily designed using a simple yet useful equation and the adapted methodology. This equation shows a voltage waveform close to the simulated one in terms of overvoltage and damping time. A snubber design is tested in both the simulation and mathematical model, showing in both cases an improvement in terms of overvoltage values and ringing. This validates the utility of this method to reduce the component voltage derating and improve the EMC compatibility. This improvement is made thanks to a 2W losses snubber with a 1 MHz switching frequency.

An application of this methodology in electrical vehicles allows for an increased working voltage for a given component while keeping the additional losses as low as possible. This then implies a higher power density saving volume for other parts of the vehicle such as batteries. The improved EMC compatibility could also help saving space and costs by having less electromagnetic shields. This methodology can be applied to both high and low voltage designs and help reaching higher switching frequencies while keeping the overshoot under control.

A functional prototype will be designed to verify how the mathematical modeling performs when compared to experimental data.

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